CLAIMS

1. A switched capacitor bandgap reference circuit comprising:

a) a first transistor adapted to operate at a first current density so as to provide a first transistor output,

b) a second transistor adapted to operate at a second current density so as to provide a second transistor output,

c) a switched capacitor amplifier including a capacitor network, the amplifier providing an output based on the difference between the first and second transistor outputs,

d) a capacitor shield adapted to shield said capacitor network, and

e) a voltage driving circuit coupled to said capacitor shield, the voltage driving circuit being adapted to drive said shield to the voltage of one of the transistor outputs.

2. The circuit as claimed in claim 1 wherein the capacitor network includes at least two capacitors, a first capacitor coupled to an inverting input of the amplifier and a second capacitor provided in a feedback loop between the output of the amplifier and the inverting input.

3. The circuit as claimed in claim 2 wherein the first and second capacitors are provided with an interconnect therebetween, the circuit additionally comprising an interconnect shield adapted to shield said interconnect and wherein the interconnect shield is also coupled to a voltage driving circuit, the voltage driving circuit being adapted to drive said shield to the voltage of one of the transistor outputs.

4. The circuit as claimed in claim 3 wherein the driving circuit coupled to the interconnect shield and the driving circuit coupled to the capacitor shield are the same.

5. The circuit as claimed in claim 3 wherein the capacitor shield and the interconnect shield are provided by the same shield.

6. The circuit as claimed in claim 1 wherein the capacitors are provided by at least two layers in a multi-layer structure, the at least two layers being formed one above the other and being separated from one another and wherein the capacitor shield is formed as a layer above the upper layer of the capacitor structure.

7. The circuit as claimed in claim 3 wherein the interconnect is provided by a layer within a multi-layer structure.

8. The circuit as claimed in claim 7 wherein the interconnect layer is provided in a sandwich arrangement, being shielded above and below by layers of the multi-layer structure.

9. The circuit as claimed in claim 7 wherein one of the layers of the multi-layer structure is used to provide an interconnect layer, the interconnect layer being shielded above and below by other layers of the multi-layer structure.

10. The circuit as claimed in claim 9 wherein two or more layers are coupled to one another, thereby being provided at the same potential, these layers providing at least one of the capacitor shield or interconnect shield.

11. The circuit as claimed in claim 3 further including a switching device coupled to the second capacitor and provided in the feedback loop between the amplifier output and its inverting input.

12. The circuit as claimed in claim 11 wherein an interconnect between the second capacitor and the switching device is also shielded with the interconnect shield.

13. The circuit as claimed in claim 12 wherein the interconnect is provided by a layer within a multi-layer structure and the shield is provided by layers above and below the interconnect layer.

14. The circuit as claimed in claim 13 wherein at least one of the layers in the multi-layer structure is a metal layer.

15. The circuit as claimed in claim 13 wherein at least one of the layers in the multi-layer structure is formed from polysilicon material.

16. The circuit as claimed in claim 1 wherein the amplifier output is a combination of a proportional to absolute temperature (PTAT) voltage provided by the difference in base emitter voltages between the two transistors and a voltage provided by the base emitter voltage of one of the transistors.

17. The circuit as claimed in claim 16 wherein the capacitor network includes a first capacitor coupled to the negative input of the amplifier and a second capacitor provided in a feedback loop between the output of the amplifier and the negative input of the capacitor and the PTAT voltage is scaled by a value proportional to the ratio of the values of the first and second capacitors.

18. The circuit as claimed in claim 17 wherein the base emitter voltage of one of the transistors includes a second order TlnT term, the TlnT term contributing a curvature effect at the output of the amplifier and wherein the circuit further includes curvature correction components, the curvature correction components adapted to provide a complimentary TlnT voltage term which is superimposed at the output of the amplifier so as to compensate for any bow effect arising from the second order TlnT term of the base emitter voltage of one of the transistors.

19. The circuit as claimed in claim 18 wherein the curvature correction components are coupled to the inverting input of the amplifier.

20. The circuit as claimed in claim 19 wherein a third capacitor is provided, the third capacitor being provided in the path between the inverting input of the amplifier and the curvature correction components.

21. The circuit as claimed in claim 20 wherein an interconnect between the third capacitor and the inverting input is shielded, the shield being coupled to a voltage driving circuit, the

voltage driving circuit being adapted to drive said shield to the voltage of one of the transistor outputs.

22. The circuit as claimed in claim 21 wherein the curvature correction components may be switchably coupled to the amplifier.

23. The circuit as claimed in claim 18 wherein the curvature correction components include a stacked transistor arrangement.

24. The circuit as claimed in claim 1 wherein the voltage driving circuit includes a transistor configured as a voltage follower, the transistor being coupled to a current source and ground, the gate of the transistor being coupled to one of the transistors operating at different current densities.

25. A switched capacitor bandgap reference circuit including an amplifier having a first capacitor coupled to its inverting input and a second capacitor provided in a feedback loop from the output to the inverting input, each of the capacitors being formed from a stack arrangement, the stack including first and second layers located one above the other and having a shield located thereabove, the circuit additionally including a first and a second bipolar transistor, the transistors adapted to operate at different current densities and being switchably coupled to the inverting and non-inverting inputs of the amplifier such that, in use, a switching operation effects the generation of a difference in base emitter voltage, ΔVeb, between the two transistors which when coupled to a base emitter voltage of the first transistor generates at the output of the amplifier a voltage reference, and wherein a voltage follower is additionally provided, the voltage follower being coupled to the shield of the capacitors and being further adapted to track voltage changes at the amplifier input, thereby bootstrapping the shield of the capacitors to the first transistor and minimizing the effect of parasitic capacitances.

26. The circuit as claimed in claim 25 wherein the voltage follower is a high impedance device.

27. The circuit as claimed in claim 25 wherein the voltage follower is provided as a MOSFET device.

28. A switched capacitor bandgap reference circuit including an amplifier having a first capacitor coupled to its inverting input and a second capacitor provided in a feedback loop from the output to the inverting input, the circuit additionally including a first and a second bipolar transistor, the transistors adapted to operate at different current densities and being switchably coupled to the inverting and non-inverting inputs of the amplifier such that, in use, a switching operation effects the generation of a difference in base emitter voltage, ΔVeb, between the two transistors which when coupled to a base emitter voltage of the first transistor generates at the output of the amplifier a voltage reference, the voltage reference being a combination of a proportional to absolute temperature (PTAT) voltage provided by the difference in base emitter voltages between the two transistors and a voltage provided by the base emitter voltage of the first transistor, the voltage provided by the base emitter voltage of the first transistor having first and second order contributions and wherein the circuit additionally comprises curvature correction components, the curvature correction components being coupled to the inverting input of the amplifier and adapted to provide a complimentary voltage to the second order contribution of the first transistor so as to compensate for any bow effect arising from the second order contribution.

29. The circuit as claimed in claim 28 wherein the ratio of the values of the first and second capacitors determines a scaling of the PTAT voltage.

30. The circuit as claimed in claim 28 wherein the curvature correction components are coupled to the inverting input via a third capacitor.

31. The circuit as claimed in claim 28 wherein the curvature correction components may be switchably coupled to the inverting input.

32. The circuit as claimed in claim 30 wherein each of the capacitors is formed in a multi-layer stack, the stack including first and second layers located one above the other and having a shield located thereabove.

33. The circuit as claimed in claim 32 additionally comprising a voltage follower, the voltage follower being coupled to the shield of the capacitors and being further adapted to track voltage changes at the amplifier input, thereby bootstrapping the shield of the capacitors to the first transistor and minimizing the effect of parasitic capacitances.

34. The circuit as claimed in claim 32 wherein an interconnect between the first, second and third capacitors is provided in a layer of the multi-layer stack, the interconnect being provided with a shield above and below the interconnect.

35. The circuit as claimed in claim 34 wherein the interconnect shield is additionally coupled to a voltage follower, the voltage follower being adapted to track voltage changes at the amplifier input, thereby bootstrapping the interconnect shield to the first transistor and minimizing the effect of parasitic capacitances.

36. The circuit as claimed in claim 28 wherein the curvature correction components include a plurality of transistors provided in a stack arrangement.